REMARKS

Claims 1-4, 11 and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by Borchers, *et al.* (U.S. Publication Number 2004/0044934). Claims 7 and 9 are rejected under 35 U.S.C. § 102(b) as being anticipated by Moloney, *et al.* (U.S. Patent Number 5,528,237). Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Borchers, *et al.* in view of Kubota, *et al.* (U.S. Patent Number 5,654,658). Claims 8 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Moloney, *et al.* in view of Kubota, *et al.* In view of the amendments to the claims and the following remarks, the rejections are respectfully traversed, and reconsideration of the rejections is requested.

The applicants' invention is directed to a circuit and method for generating control signals used in controlling memory access through memory addressing. One of the control signals is a column latch signal COLLAT, and the other signal is a data input/output command signal COLCYC. The column latch signal COLLAT is output at a first output terminal of the circuit, and the data input/output command signal COLCYC is output at a second output terminal of the circuit. A series of latches and a selection circuit, such as a multiplexer circuit, are used to generate the control signals in response to a clock signal. In response to a test enable signal in a first state, the two control signals COLLAT and COLCYC are output separated by a first time interval, and, in response to the test enable signal being in a second state, the two control signals are output separated by a second time interval. The two time intervals are controlled in units of bit time of the clock signal, and the second time interval is controlled to be smaller than the first time interval. Accordingly, in a normal operational mode, the data input/output command signal COLCYC is activated a time 2tCK after activation of the column latch signal COLLAT, where tCK is the period of the clock signal. In a test mode, the data input/output command signal COLCYC is activated after 1tCK after activation of the column latch signal COLLAT.

The claims are amended to clarify certain features of the invention. Specifically, the claims are amended to clarify that the column latch signal is a control signal coupled between the control generation circuit of the invention and a memory circuit and is used to latch a column address for accessing the memory circuit. The claims are also amended to clarify that the data

input/output command signal is a control signal coupled between the control signal generation circuit of the invention and the memory circuit and is used to control data read and write operations on a selected column of the memory circuit. It is believed that these amendments to the claims clarify the distinctions between the claimed invention and the cited references.

The Borchers, *et al.* reference is directed to a circuit for generating an error bit to indicate errors in a memory. Referring to the Figure in Borchers, *et al.*, the circuit is used to test the integrity of a sequential device such as a memory 2. A test output signal 4 from the memory circuit is generated to alternately toggle on edges of the clock input signal 3. The output signals from flip-flops 7 and 8 are sent to a multiplexer 13 which selects one of the outputs based on the state of a selection line 14. The output of the multiplexer is sent to the input of an exclusive OR gate 16. The output of the flip-flop 9 is also applied to the input of the exclusive OR gate 16. The error signal at the output 23 of latch L2 is preset to an inactive state by preset line 15. When the two inputs to the exclusive OR gate 16 are the same, the output of the exclusive OR gate 16 is active such that the D input to latch L2 remains active, such that the error signal remains inactive. The inactive error signal indicates that the data output 4 from the memory 2 is toggling. When the two inputs to the exclusive OR gate 16 are not the same, indicating that the data output 4 from the memory 2 is not toggling, the error signal 23 becomes active.

Hence, Borchers, *et al.* discloses an error detection circuit which produces an error output during testing of a sequential device such as a memory circuit. This is in contrast to the applicants' claimed invention, in which control signals are generated to control access to a memory, as set forth in the amended claims. Specifically, Borchers, *et al.* do not teach or suggest a column latch signal coupled between a control signal generation circuit and a memory circuit used to latch a column address for accessing the memory circuit. Borchers, *et al.* also do not teach or suggest a data input/output command signal between the control signal generation circuit and the memory circuit used to control data read and write operations on a selected column of the memory circuit. This follows, since, for example, Borchers, *et al.* teach a circuit that receives a signal from a memory circuit 2. Borchers, *et al.* do not teach or suggest generating control signals that are sent to a memory circuit, as the applicants claim. The details of these control

circuits set forth in the amended claims are neither taught nor suggested by Borchers, *et al.*

Borchers, *et al.* fail to teach or suggest the invention set forth in the amended claims. Accordingly, it is believed that the amended claims are allowable over Borchers, *et al.* Accordingly, reconsideration of the rejections of claims 1-4, 11 and 12 under 35 U.S.C. § 102(e) based on Borchers, *et al.* is respectfully requested.

Kubota, *et al.* is cited as teaching a flip-flop circuit that is capable of operating at a high operation speed. However, Kubota, *et al.* fail to teach or suggest the elements of the amended claims absent from Borchers, *et al.* discussed above. That is, Borchers, *et al.* fail to teach or suggest the applicants' claimed column latch signal and data input/output command signal used in controlling operations of a memory circuit. Since neither of Borchers, *et al.* and Kubota, *et al.* teach or suggest these features of the invention set forth in the amended claims, there is no way to combine the two references to obtain such teaching or suggestion. Therefore, it is believed that the claims are allowable over the combination, and reconsideration of the rejection of claims 5 and 6 under 35 U.S.C. § 103(a) based on Borchers, *et al.* and Kubota, *et al.* is respectfully requested.

Like Borchers, *et al.*, Moloney, *et al.* also fail to teach or suggest a circuit and method for generating control signals used in controlling access to a memory circuit. Specifically, Moloney, *et al.* do not teach or suggest a column latch signal coupled between a control signal generation circuit and a memory circuit used to latch a column address for accessing the memory circuit. Likewise, Moloney, *et al.* also fail to teach or suggest a data input/output command signal coupled between the control signal generation circuit and the memory circuit used to control data read and write operations on a selected column of the memory circuit. Since Moloney, *et al.* fail to teach or suggest the invention set forth in the amended claims, it is believed that the claims are allowable over Moloney, *et al.* Accordingly, reconsideration of the rejections of claims 7 and 9 under 35 U.S.C. § 102(b) based on Moloney, *et al.* is respectfully requested.

As noted above, Kubota, *et al.* also fails to teach or suggest the elements of the invention discussed above and set forth in the amended claims. Accordingly, there is no combination of Moloney, *et al.* with Kubota, *et al.* that would result in providing such teaching or suggestion.

Accordingly, it is believed that the claims are allowable over the combination of Moloney, *et al.* and Kubota, *et al.* Therefore, reconsideration of the rejections of claims 8 and 10 under 35 U.S.C. § 103(a) based on Moloney, *et al.* and Kubota, *et al.* is respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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